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EXAMINER

PETRANEK, JACOB ANDREW

ART UNIT

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/531,610	<b>Applicant(s)</b> REGNIER, LAURENT	
	<b>Examiner</b> Jacob Petranek	<b>Art Unit</b> 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 14 November 2008.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

**DETAILED ACTION**

1. Claims 1-20 are pending.
2. The office acknowledges the following papers:  
Claims and arguments filed on 11/14/2008.

***New Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:  
  
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
4. Claims 1-20 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 7-8 recite “substantially simultaneously with storing.” The term substantially is indefinite and it cannot be determined what the metes and bounds of the term are.

5. Claims 2-6 and 9-20 are rejected due to their dependency.

***New Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 8 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita (U.S. 6,467,083), in view of Trauben (U.S. 5,594,864).

8. As per claim 8:

Yamashita disclosed a method for monitoring a microprocessor executing a sequence of instructions by means of a device integrated to a microprocessor chip, the method comprising:

on each execution of an instruction from the sequence of instructions, generating a digital message of a type corresponding to a type of the executed instruction (Yamashita: Figure 3 element 22, column 8 lines 9-26)(Information of the executed instruction codes and status of the instruction codes are passed from the data selector to the trace generator to generate trace packets. The trace generator generates a plurality of different trace packets.); and

storing each generated digital message in a buffer memory (Yamashita: Figure 3 element 17, column 8 lines 27-38); and

an output terminal (Yamashita: Figure 3 element 24) connected to an external analysis tool (Yamashita: Figure 3 element 13).

Yamashita failed to teach modifying a state of an output terminal associated with an instruction type from the sequence of instructions substantially simultaneously with storing in the buffer memory, at a storage time, a digital message of a type corresponding to the instruction type, wherein the output terminal associated with the instruction type is from a plurality of output terminals connected to an external analysis

tool, with each output terminal from the plurality of output terminal being associated with an instruction type from the sequence of instructions.

However, Trauben disclosed modifying a state of an output terminal associated with an instruction type from the sequence of instructions substantially simultaneously with storing in the buffer memory, at a storage time, a digital message of a type corresponding to the instruction type (Trauben: Figure 5 element 51, column 8 lines 26-30)(Yamashita: Figure 3 elements 17 and 23, column 8 lines 27-38)(The combination results in the plurality of output pins being used in place of the single output terminal to the emulator of Yamashita. The output pins of Trauben are changed on a cycle-by-cycle basis to provide information about the processor's execution. It's obvious to one of ordinary skill in the art that a trace packet for a given instruction type can be stored in the same clock cycle as an output pin is asserted for a trace packet of the given instruction type.), wherein the output terminal associated with the instruction type is from a plurality of output terminals connected to an external analysis tool (Trauben: Figure 5 element 51, column 8 lines 48-67 continued to column 9 lines 1-7)(There are a plurality of output terminals, where at least one of which is associated with an instruction type.), with each output terminal from the plurality of output terminal being associated with an instruction type from the sequence of instructions (Trauben: Figure 5 element 51, column 8 lines 48-67 continued to column 9 lines 1-7)(All of the terminals are associated with instruction types.).

The advantage of using a plurality of terminals in Trauben is that it allows the observation of important processor internal states in a cycle-by-cycle basis (Trauben:

Column 8 lines 26-30). One of ordinary skill in the art would have been motivated by this advantage to implement the plurality of output terminals into the processor of Yamashita. Thus, one of ordinary skill in the art at the time of the invention to implement the output terminals of Trauben into the processor of Yamashita for the advantage of allowing observation of internal states in a cycle-by-cycle basis.

9. As per claim 20:

The additional limitation(s) of claim 20 basically recite the additional limitation(s) of claim 18. Therefore, claim 20 is rejected for the same reason(s) as claim 18.

10. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita (U.S. 6,467,083), in view of Trauben (U.S. 5,594,864), further in view of Chen et al. (U.S. 5,642,478).

11. As per claim 9:

The additional limitation(s) of claim 9 basically recite the additional limitation(s) of claim 2. Therefore, claim 9 is rejected for the same reason(s) as claim 2.

12. Claims 1, 3, 5-7, 11-14, and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita (U.S. 6,467,083), in view of Trauben (U.S. 5,594,864), in view of Edwards et al. (U.S. 6,918,065).

13. As per claim 1:

Claim 1 essentially recites the same limitations of claim 8. Claim 1 additionally recites the following limitations:

Yamashita and Trauben failed to teach to indicate to the external analysis tool a storage time.

However, Edwards disclosed to indicate to the external analysis tool a storage time (Edwards: Figure 7 element 708, column 12 lines 29-35)(The combination with Yamashita results in trace messages with timestamps, that are passed via an output terminal to the external analysis tool.).

The advantage of using timestamps is that trace data generated by different functional units can be temporally correlated to properly debug a processing system. One of ordinary skill in the art would have been motivated by this advantage to implement trace timestamps onto the processor of Yamashita. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement timestamps in the processor of Yamashita for the advantage of being able to temporally correlate traces between different functional units.

14. As per claim 3:

Yamashita, Trauben, and Edwards disclosed the monitoring device of claim 1, wherein each output terminal (Trauben: Figure 5 element 51) is connected to a test terminal (Trauben: Figure 5 element 55, column 8 lines 23-26).

15. As per claim 5

Yamashita, Trauben, and Edwards disclosed the monitoring device of claim 1, wherein only certain types of instructions only are associated with an output terminal of the message calculation means (Trauben: Figure 5 element 51, column 8 lines 48-

50)(Only certain instructions will cause a message to be output via the output terminals.).

16. As per claim 6:

Yamashita, Trauben, and Edwards disclosed the monitoring device of claim 1, wherein each of the predetermined instruction types is associated with an output terminal of the message calculation means (Trauben: Figure 5 element 51, column 8 lines 48-50)(Only certain instructions will cause a message to be output via the output terminals. However, it's obvious to one of ordinary skill in the art that additional output terminals could be added so that all instruction types can be monitored for the advantage of being able to monitor all instructions executing in a program.).

17. As per claim 7

Claim 7 essentially recites the same limitations of claim 1. Claim 7 additionally recites the following limitations:

a microprocessor for executing a sequence of instructions (Yamashita: Figure 3 element 15, column 7 lines 26-39).

18. As per claim 11:

The additional limitation(s) of claim 11 basically recite the additional limitation(s) of claim 3. Therefore, claim 11 is rejected for the same reason(s) as claim 3.

19. As per claim 12:

Yamashita, Trauben, and Edwards disclosed the integrated circuit of claim 11, wherein a state of the test terminal is modified when a state of the output terminal connected to the test terminal is modified (Trauben: Figure 5 elements 51 and 55,

column 8 lines 23-26)(A change occurs at element 55 after a change occurs at element 51.).

20. As per claim 13:

Yamashita, Trauben, and Edwards disclosed the integrated circuit of claim 7, wherein, when at least two instructions of a first and a second type from the sequence instructions are executed in parallel (Trauben: Column 4 lines 32-41), the message calculation means generates a digital message corresponding to an instruction of a first type and modifies a state of an output terminal associated with the instruction of the first type and simultaneously generates a digital message corresponding to an instruction of a second type and modifies a state of an output terminal associated with the instruction of the second type (Trauben: Figure 5 element 51, column 4 lines 32-41 and column 8 lines 27-30)(The processor generates digital messages on the state of the processor on a cycle-by-cycle basis. The processor is also superscalar and is able to issue a plurality of instructions per cycle. Thus, it's obvious to one of ordinary skill in the art that since multiple types of instructions can be issued per cycle, multiple messages can be generated per cycle.).

21. As per claim 14:

Yamashita, Trauben, and Edwards disclosed the integrated circuit of claim 13, wherein the external analysis tool stores a time when the state of the output terminal associated with the instruction of the first type was modified and a time when the state of the output terminal associated with the instruction of the second type was modified (Edwards: Figure 7 element 708, column 12 lines 29-35)(The combination with

Yamashita results in trace messages with timestamps, that are passed via an output terminal to the external analysis tool. This results in traces for a plurality of different types of instructions having timestamps with their corresponding trace data.).

22. As per claim 16:

Yamashita, Trauben, and Edwards disclosed the integrated circuit of claim 7, wherein each output terminal from the plurality of output terminals is associated with a plurality of instruction types (Trauben: Figure 5 element 51, column 8 lines 48-50)(Only certain instructions will cause a message to be output via the output terminals.

However, it's obvious to one of ordinary skill in the art that output terminals could be asserted for a plurality of instruction types for the advantage of being able to monitor all instructions executing in a program without having to add additional output terminals or to eliminate some output terminals. The advantage of eliminating output terminals is that costs are reduced.).

23. As per claim 17:

The additional limitation(s) of claim 17 basically recite the additional limitation(s) of claim 6. Therefore, claim 17 is rejected for the same reason(s) as claim 6.

24. As per claim 18:

Yamashita, Trauben, and Edwards monitoring device of claim 1, wherein the plurality of output terminals are connected to the external analysis via a plurality of test terminals (Trauben: Figure 5 element 51, column 8 lines 48-50)(The test terminals are the connections between the testing device and the external analysis tool

in figure 1 of the application drawings. Thus, the pipe reads on the test terminals between the output of the CPU and the logic analyzer.),

each output terminal from the plurality of output terminals is connected to a test terminal from the plurality of test terminals (Trauben: Figure 5 element 51, column 8 lines 48-50)(Each output pipe signal from the CPU is connected to element 51), and

a state of the test terminal is modified when a state of the output terminal connected to the test terminal is modified (Trauben: Figure 5 element 51, column 8 lines 48-50)(It's obvious to one of ordinary skill in the art that the pipe element 51 is modified when the corresponding output is modified.).

25. As per claim 19:

Yamashita, Trauben, and Edwards monitoring device of claim 1, wherein, when at least two instructions of a first and a second type from the sequence instructions are executed in parallel (Yamashita: Figure 3 element 15)(Official notice is given that processors can execute instructions in parallel in a superscalar manner. Thus, it's obvious to one of ordinary skill in the art that the CPU is a superscalar processor that executes instructions in parallel.), the message calculation means generates a first digital message corresponding to an instruction of a first type and modifies a state of art output terminal associated with the instruction of the first type substantially simultaneously with storing the first digital message in the buffer memory and simultaneously generates a second digital message corresponding to an instruction of a second type and modifies a state of an output terminal associated with the instruction of the second type substantially simultaneously with storing the second digital message in

the buffer memory (Trauben: Figure 5 element 51, column 8 lines 26-30)(Yamashita: Figure 3 elements 17 and 23, column 8 lines 27-38)(The combination results in the plurality of output pins being used in place of the single output terminal to the emulator of Yamashita. The output pins of Trauben are changed on a cycle-by-cycle basis to provide information about the processor's execution. It's obvious to one of ordinary skill in the art that a trace packet for a given instruction type can be stored in the same clock cycle as an output pin is asserted for a trace packet of the given instruction type.).

26. Claims 2 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita (U.S. 6,467,083), in view of Trauben (U.S. 5,594,864), in view of Edwards et al. (U.S. 6,918,065), further in view of Chen et al. (U.S. 5,642,478).

27. As per claim 2, the rejection of claim 1 is incorporated and:

Yamashita, Trauben, and Edwards disclosed the monitoring device of claim 1.

Yamashita, Trauben, and Edwards failed to teach the buffer memory is divided into a plurality of areas, each of the areas is associated with a different instruction type and is intended to only store messages associated with said instruction type.

However, Chen disclosed the buffer memory (Chen: Figure 1 element 32) is divided into a plurality of areas (Chen: Figure 1 element 56), each of the areas is associated with a different instruction type and is intended to only store digital messages associated with said instruction type (Chen: Column 9 line 23-26)(Each divided buffer space stores traces for only a certain type or types of instructions.).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include different areas in the buffer memory and each associated to each instruction type in the system of Yamashita and Trauben because Chen teach that the inclusion would enable the correlation of trace data from different source(Chen Column 9 line 1-2). It enhances the capability of the accumulation of trace data information by organization of the information in the storage (Yamashita column 5 line 21-24).

28. As per claim 10:

The additional limitation(s) of claim 10 basically recite the additional limitation(s) of claim 2. Therefore, claim 10 is rejected for the same reason(s) as claim 2.

29. Claims 4 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita (U.S. 6,467,083), in view of Trauben (U.S. 5,594,864), in view of Edwards et al. (U.S. 6,918,065), further in view of Mihalik et al. (U.S. 4,574,354).

30. As per claim 4:

Yamashita, Trauben, and Edwards disclosed the monitoring device of claim 1.

Yamashita, Trauben, and Edwards failed to teach each output terminal is connected to an input terminal of a coding block comprising a predetermined number of coding block output terminals, each of the coding block output terminals is connected to a test terminal, each coding block being provided to have each of its n coding block output terminals switch once every n state switchings of its input terminal and so that a single one of its n coding block output terminals switches state at once.

However, Mihalik discloses each output terminal (Mihalik: Figure 1 element 12C) is connected to an input terminal of a coding block (Mihalik: Figure 1 element 16) comprising a predetermined number of coding block output terminals, each of the coding block output terminals is connected to a test terminal (Mihalik: Figure 1 element 14, column 7 lines 53-57)(Each bit of the output of a grey code counter is an output terminal of the coding block.), each coding block being provided to have each of its n coding block output terminals switch once every n state switchings of its input terminal (pulse emitted by TTA) and so that a single one of its n coding block output terminals switches state at once [the use Grey code (column 7 line 53-57)].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include encode state change in the output terminal by Gray code to be a encoded number in the system of Yamashita and Trauben because it is encoded the number of the time the state of input terminal change into a count (Mihalik column 7 line 53-57). It enhances the capability of the accumulation of trace data information by collecting more information (the count of certain type of instruction executed in the processor) (Yamashita column 5 line 21-24).

31. As per claim 15:

The additional limitation(s) of claim 15 basically recite the additional limitation(s) of claim 4. Therefore, claim 15 is rejected for the same reason(s) as claim 4.

### ***Response to Arguments***

32. The arguments presented by Applicant in the response, received on 11/14/2008 are not considered persuasive.

33. Applicant argues "On page 12, the Office Action indicates that "an amendment stating that a given message is stored and outputted via an output terminal simultaneously would overcome the current rejections." Claim 8 has been amended to recite modifying a state of an output terminal associated with an instruction type from the sequence of instructions substantially simultaneously with storing in the buffer memory, at a storage time, a digital message of a type corresponding to the instruction type, wherein the output terminal associated with the instruction type is from a plurality of output terminals connected to an external analysis tool, with each output terminal from the plurality of output terminals being associated with an instruction type from the sequence of instructions (emphasis added). None of the cited reference teaches or suggests this limitation" for claims 1, 7, and 8.

This argument is not found to be persuasive for the following reason. The examiner agrees that an amendment stating a given message is stored and outputted via an output terminal simultaneously would overcome the rejections. However, this isn't quite claimed yet. The current claims allow for a given message type to be stored and outputted simultaneously. The combination can read upon this claimed limitation by having two messages of the same type be stored and outputted in a given processing cycle. Specifically, a given message can be outputted from elements 23 and 24 in figure 3 of Yamashita in the same processing cycle, which reads upon the newly claimed limitations.

The examiner notes that an amendment stating that a given message (i.e. a single message of a given type) is stored and outputted via an output terminal simultaneously would overcome the current rejections. This appears to be shown in figure 2 by elements 28-32 (output terminals) and 34 (buffer memory).

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Eddie P Chan/  
Supervisory Patent Examiner, Art Unit 2183

Jacob Petranek  
Examiner, Art Unit 2183